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EIC Detector R&D Progress Report

Project ID: eRD18
Project Name: Precision Central Silicon Tracking & Vertexing from the EIC
Period Reported: October 1 to December 31, 2016
Project Leader: Peter G. Jones
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Abstract

We propose to develop a detailed concept for a central silicon pixel detector for an Electron-Ion Collider at BNL or JLab exploring the advantages of using HV-CMOS or HR-CMOS MAPS technologies. The sensor development will exploit the newly created Birmingham Instrumentation Laboratory for Particle Physics and Applications. An accompanying simulation study will optimise the basic layout, location and sensor/pixel dimensions to find the best achievable momentum resolution and vertex reconstruction resolution. This initial design study will allow future full-detector simulations to explore precision measurements of heavy flavour processes and scattered electrons at high Q^2.

1. Past

What was planned for this period?

This project is just starting. The panel recommended that we focus on WP1: Sensor Development and WP2: Silicon Detector Layout Investigations. The plan for this period was to recruit a postdoc who will perform the simulation work and assist with the sensor testing at a later stage of the project. We have identified a candidate for the position and the contract negotiation with BNL is underway. We expect to be in a position to make an appointment by the end of January or early February. The simulation effort will start in earnest in the next reporting period.

We report here on the progress made on WP1. The primary goal of WP1 is to demonstrate improved spatial resolution by means of fast charge collection in a large depleted sensor volume with MAPS detectors fabricated in commercial CMOS technologies featuring high voltage and high resistivity substrates. We planned to submit test structures in two technologies to investigate their charge collection properties on the timescale of early-mid 2017.

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What was achieved?

One technology we propose to investigate is the HR-CMOS variant of the TPSCo 180 nm process used in the current state-of-the-art ALPIDE MAPS detectors being developed by ALICE. Access to this technology is available via two routes. As written in the original proposal, we are working in collaboration with colleagues from RAL and Sussex University on an STFC-funded PRD for the design of radiation-hard, reconfigurable MAPS detectors for outer tracking and digital electromagnetic calorimeters. The second is via recent synergies emerging with the CERN groups working on the TPSCo technology for the development of more radiation-hard depleted MAPS for the ATLAS pixel detector at the HL-LHC.

For the first project, the so-called DECAL MAPS, the same TPSCo process as the ALICE ITS pixel design is used. The possibility of increasing depletion by moving the junction to the substrate contact with the epitaxial layer, as originally proposed, has been ruled out by measurements on existing test structures. Results show that more work on the process in collaboration with TPSCo would be needed, which cannot be done with the available resources of the DECAL-MAPS project. We thus aim to achieve larger depletion with a different configuration of the diode. TCAD simulations carried out so far show that a configuration with multiple diodes in the pixel would provide increased depletion. The resulting increase in detector capacitance has yet to be estimated. Specifications for the chip have been defined and preliminary pixel schematics and layout are well underway. The pixel size will have to be 60 x 60 μm^2 to satisfy the requirements of the DECAL-MAPS project. Test structures with smaller pixel pitch will be implemented if space is available after design of the DECAL-MAPS chip is completed.

Collaboration starting with the CERN groups working on TPSCo will allow us to submit test structures in a modified version of the process where larger depletion has been demonstrated for a configuration with one small collection electrode as in the ALPIDE MAPS detector. In the modified process, developed by TPSCo in collaboration with CERN, the depletion region reaches below the deep p-well containing the electronics thanks to the development of a planar junction within the epitaxial layer (as opposed to at the interface to the substrate, as in our original proposal where this new technology option had not been available). We will also have access to the testing of an existing demonstrator chip produced with the modified TPSCo process containing a number of pixel matrices with different diode layout and pixel pitch ranging from 20 x 20 μm^2 to 50 x 50 μm^2.

The second technology is the LFoundry 150 nm quadruple well process, which we can access via our membership of the RD50 collaboration. Together with other institutes from the collaboration we are preparing a submission of both active and passive test structures in this technology. The preliminary macro layout includes five active pixel matrices with improved timing performance (Time-Of-Amplitude and Time-to-Digital-Conversion among others), and a number of passive test structures for TCT tests and capacitance measurements. The aim is to design the pixels with the smallest achievable pitch, possibly well below 50 x 50 μm^2. Different sizes and

layout of the collection electrode will also be investigated. We have also signed a non-disclosure agreement with LFoundry so that we can now acquire process information to start TCAD simulations.

Both submissions are foreseen for late spring 2017.

What was not achieved, why not, and what will be done to correct?

We believe that the project is on track at this stage.

2. Future

What is planned for the next funding cycle and beyond? How, if at all, is this planning different from the original plan?

During the second half of the current funding cycle, January-July 2017, we will begin work on the detector layout simulations (WP2). The plan is to work within existing simulation frameworks, such as EIC-ROOT, but maintaining an ability to adopt current and future software developments, particularly a common geometry and detector interface to simulations.

We will complete the test structure submissions (WP1) as outlined above.

What are critical issues?

Postdoc retention and continuity of funding is our main concern at this time.

Additional information:

In response to the feedback we received on our original proposal, we would like to clarify why we aim to study the effects of total ionising dose (TID) on the electronic circuits within the MAPS via dedicated irradiation campaigns at the MC40 cyclotron in Birmingham. ASICs designed in commercial deep sub-micron CMOS technologies and operating in radiation environments are affected by the "Radiation Induced Narrow Channel Effect" or RINCE [1], at doses around 1 Mrad (relatively low for vertex detectors at colliders). This is a fundamental CMOS damage mechanism, not peculiar to any vendor or foundry. It affects transistor parameters such as leakage current and threshold voltage, due to charges trapped in the oxides and at the oxide-silicon interfaces following exposure to ionising radiation. As shown in ref. [2], RINCE has been observed in 130 nm CMOS technologies from different vendors.

Processes used for CMOS active pixel devices are no exception, as shown in ref. [3], where the TID response of the electronics in a prototype HV-CMOS chip using the XFAB 180 nm SOI process shows the same effect. Processes used for HV-/HR-CMOS chips are in fact nothing else than the commercial deep sub-micron CMOS technologies used for ASICs design, with added features such High Voltage capability and/or High Resistivity substrates, to allow for sensor substrate depletion.

Although TID effects are qualitatively similar for different technologies, large quantitative differences arise depending on the oxide processing and doping profile of the substrate. These can also arise for the same technology from lot to lot, if any change is applied to the process. Whilst it is true that design guidelines exist to mitigate the phenomenon, the technologies should be monitored constantly as a change in the process, normally not communicated by the vendor, could change drastically the TID response of the transistors.

We thus believe that dedicated irradiation campaigns to test the TID performance of prototype MAPS detectors are mandatory and groups working on these technologies are integrating transistor test structure in their MAPS prototype to carry out these studies. As these effects are in fact most prominent for relatively low TID (1-2 Mrad), irradiations need to be performed in small TID steps. A proton irradiation to fluences typical of high luminosity experiments (10^{14} – 10^{16} 1MeV n_{eq}/cm^2), corresponding to high TID, would in fact not show whether any TID induced RINCE effect is present.

[1] F. Faccio, G. Cervelli, Radiation-induced edge effects in deep submicron CMOS transistors, IEEE Transactions on Nuclear Science, Vol. 52, No. 6, December 2005
[2] L. Gonella, F. Faccio et al., Total ionizing dose effects in 130 nm commercial CMOS technologies for HEP experiments, Nucl. Instrum. Meth. A582 (2007) 750-754, DOI: 10.1016/j.nima.2007.07.068
[3] S. Fernandez-Perez et al., Radiation hardness of a 180 nm SOI monolithic active pixel sensor, Nucl. Instrum. Meth. A796 (2015) 13-18, DOI: 10.1016/j.nima.2015.02.066

3. Manpower

Include a list of the existing manpower and what approximate fraction each has spent on the project. If students and/or postdocs were funded through the R&D, please state where they were located and who supervised their work.

Prof. Peter Jones (0.05 FTE) – no cost to project
Dr. Laura Gonella (0.2 FTE) – no cost to project
Prof. Phil Allport and Prof. Paul Newman have had an advisory role and participate in our regular project meetings to monitor progress.
Postdoctoral Researcher – (0.5 FTE) – funded by EIC funds, to start in 2017.

4. External Funding

Describe what external funding was obtained, if any. The report must clarify what has been accomplished with the EIC R&D funds and what came as a contribution from potential collaborators.

EIC R&D funds support a junior postdoctoral researcher at 0.5 FTE per year. It is a priority for us to seek matching funds from other sources. We have already applied for matching funds as part of our next 4-year Nuclear Physics Consolidated Grant, the outcome of which will be known in the summer. We also intend to bid for UK R&D funds through the STFC Project Research and Development (PRD) scheme. A

call for proposals is expected later this year with an anticipated July submission date. Successful applications will start no earlier than April 1, 2018.

5. Publications

Please provide a list of publications coming out of the R&D effort.

Not applicable at this early stage of the project.